REMARKS

Status Summary

In this amendment, no claims are added and claims 1-14, 17-24, 27-30, 32-33, 35-37, and 40 are cancelled. Therefore, upon entry of this amendment, claims 15-16, 25-26, 31, 34, 38-39, and 41-50 will be pending.

Telephone Examiner Interview Summary

Applicants greatly appreciate the telephone examiner interview granted them on November 17, 2008. In the telephone examiner interview, the fact that the product by process claims imply structural elements was discussed. Applicants agreed to present an argument as to why the elements of the product by process claims constitute structural elements. Applicants have presented such a position in the remarks below.

Applicants also agreed to make minor amendments to proposed claims 15 and 16 to be consistent with Figure 1E. Claims 15 and 16 have been amended to recite an etching step to form the channels between sidewalls of one of the first and second masking materials.

Applicants also agreed to amend claim 26 to recite elements f, g, and h, rather than a, b, and c as currently proposed. Claim 26 has been amended as proposed.

The examiner is encouraged to call Applicants' representative at the time of consideration of the amendments described herein to avoid issuance of another office action. Applicants' representative, Gregory A. Hunt, can be reached at 919-493-8000.

Claim Objections

Claims 15, 16, 25, 26, and 31 were objected to as being dependent from withdrawn claims. Claims 15, 16, and 25 have been rewritten in independent form. Claim 26 has been amended to depend from claim 25. Claim 31 depends from claim 15. Accordingly, none of these claims depend from a withdrawn claim, and the objection should be withdrawn.

Claim Rejections 35 U.S.C. §102

Claims 15, 25, 26, 31, 39, and 40 were rejected under 35 U.S.C. §102(b) as anticipated by U.S. Patent No. 6,291,137 to Lyons et al. (hereinafter, "Lyons"). This rejection is respectfully traversed.

In the Office Action, on page 3, the following is indicated:

> Furthermore, patentability of a product does not depend on its method of production. "If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."
>
> *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

It is well settled that the structure implied by process steps should be considered when assessing the patentability of product by process claims over the prior art. (See M.P.E.P. §2113.) In claims 15 and 16, the recitation of "edge-defined" as a structural element of the sidewalls in combination with the edge definition lithography steps should be treated as a structural element of the claims, similar to "welded," "press fitted," and "etched," which are recognized as structural limitations of product by process claims in M.P.E.P section 2113. Accordingly, it is respectfully submitted that "edge-defined" and "edge definition lithography" in the claims should be considered as claim elements for purposes of determining patentability over the cited art.

Claims 15 and 31

As indicated above, claim 15 has been rewritten in independent form to include all of the elements of claim 1. Claim 15 recites a system comprising a plurality of multi-periodic nanometer-scale semiconductor devices formed using the steps from claim 1. Claim 15 has further been amended to recite that each of the semiconductor devices includes at least some of the adjacent, edge-defined, nanometer-pitched sidewalls that form the nanometer-pitched channels. Thus, claim 15 recites semiconductor or electromechanical devices with plural edge-defined,

nanometer-pitched sidewalls that form plural nanometer-pitched channels in the substrate.

There is absolutely no disclosure, teaching, or suggestion in Lyons of a semiconductor structure that includes plural nanometer-pitched channels formed by adjacent nanometer-pitched sidewalls of alternating masking material. The process and the semiconductor structure described in Lyons forms only a single sidewall formed by conductive film **12** and sidewall film **18a**. (See Figure 5 of Lyons.) Because Lyons discloses a structure and a process for forming only a single sidewall and no channels, it is respectfully submitted that the rejection of independent claim 15 and dependent claim 31 as anticipated by Lyons should be withdrawn.

Claim 16

Claim 16 was not rejected based on prior art in the office action. Claim 16 has been re-written in independent form and amended to recite plural edge-defined, nanometer-pitched sidewalls similarly to claim 15. Accordingly, it is respectfully submitted that claim 16 is patentable over the documents cited in the office action for the same reasons as claim 15.

Claims 25 and 26

Independent claim 25 has been rewritten in independent form to include all of the elements of claim 17. Claim 25 recites that semiconductor device is formed by forming a sidewall of a first masking material on a substrate. An example of the sidewall of the first masking material is sidewall **400** illustrated in Figure 8. Claim 25 further recites that a second masking material is deposited on the substrate such that the second masking material covers the first sidewall with a first thickness and forms second and third sidewalls on first and second sides of the first sidewall of the second thickness being less than the first thickness. The masking material covers the substrate adjacent to the second and third sidewalls with the first thickness. As illustrated in Figure 4A, substrate **108** covers sidewall **400** and substrate **100** adjacent to sidewall **400**. Portions of the second and third sidewalls are etched from the substrate such that the first and second sides of the first sidewall form

discontinuities in the second masking material. For example, as illustrated in Figure 4B, when the sidewalls of material **108** are removed, discontinuities in masking material **108** are present on the sides of sidewall **400**. Claim 25 also recites that the first sidewall is removed from the substrate to leave a channel in the second masking material having the same width as the first sidewall. In Figure 4C, channel **402** has a width that corresponds to sidewall **400**. Claim 25 also recites that a channel is etched in the substrate corresponding to the channel in the second masking material. As illustrated in Figure 4E, channel **404** is etched in substrate **100**.

As indicated above, it is well settled that the structure implied by process steps should be considered when assessing the patentability of product by process claims over the prior art. (See M.P.E.P. §2113.) In claim 25, the process steps not only imply structure, they explicitly recite structure, i.e., a channel formed in the substrate by the selective etching and removal of a sidewall. Accordingly, it is respectively submitted that the channel and its formation steps constitute claim elements of claim 25 should be considered for patentability. In order to clarify that the channel constitutes part of the claim, claim 25 has been amended to recite that the semiconductor device includes the channel.

As stated above with regard to the rejection of claim 15, Lyons fails to disclose the formation of any channel and its substrate. According to Lyons, the technique described therein forms a single sidewall only. A single sidewall cannot form a channel as claimed. Accordingly, the rejection of 25 and dependent claim 26 as anticipated by Lyons should be withdrawn.

Claims 39 and 40

Independent claim 39 recites a semiconductor structure including at least one micrometer-scale feature and at least one nanometer-scale feature defined using edge definition lithography. Claim 39 recites a semiconductor substrate and at least one micrometer-scale feature being located in or on the semiconductor substrate. Claim 39 further recites at least one nanometer-scale feature being located in or on the micrometer-scale feature where the nanometer-scale feature is defined using definition lithography. Claim 39 has been amended to recite that the micrometer-

scale feature comprises a channel formed in the substrate and a nanometer-scale feature comprises a sidewall located in the channel. Support for the amendment to claim 39 is found, for example, in Figure 8A in the present specification.

As stated above with regard to the rejection of claim 15, the only nanometer-scale feature disclosed in Lyons is a sidewall. According to Lyons, the sidewall is formed on the substrate. There is absolutely no disclosure in Lyons of forming a sidewall in a channel using edge definition lithography. Accordingly, it is respectfully submitted that the rejection of claim 39 as anticipated by Lyons should be withdrawn.

Claim 40 has been canceled. Accordingly, the rejection of this claim is now moot.

Claims Rejections 35 U.S.C §103

Claims 34-38 and 44-49 are rejected as unpatentable over U.S. Patent No. 6,242,293 to Danzilio (hereinafter, "Danzilio") in view of Lyons. This rejection is respectfully traversed.

Claims 34-38

Independent claim 34 recites a semiconductor structure having an edge-defined, nanometer-pitched feature. Independent claim 34 further recites a substrate comprising layers formed of different semiconductor materials. Claim 34 has been amended to recite the feature comprises a nanometer-pitched channel formed a masking material on a substrate. A channel is formed by edge definition lithography.

As stated above, there is no disclosure in Lyons of forming a channel using edge definition lithography. The only structure formed in Lyons is a single sidewall. Danzilio discloses a recess formed in layers **407** and **408** of a semiconductor device. (See figure 4 of Danzilio.) However, Danzilio specifically states that the recess is formed by etching down to an etch stop layer. Etching down to an etch stop layer is not edge definition lithography as claimed because etching down to the stop layer does not form sidewalls using edges as claimed. (See column 5, lines 50-67 of Danzilio.) Thus, because neither Lyons nor Danzilio teaches forming a recess in a masked material on a substrate using edge definition lithography as claimed, it is

respectfully submitted that the rejection of claim 34 and dependent claim 38 as unpatentable over Danzilio in view of Lyons should be withdrawn.

Claims 35-37 have been canceled. Accordingly, the rejection of these claims is now moot.

Claims 44-49

Independent claim 44 recites a field effect transistor having an edge defined gate. Claim 44 further recites that the filed effect transistor includes a substrate including a buffer layer of first semiconductor material and a channel layer of second semiconductor material where the two materials are different. Claim 44 further recites a gate electrode located on a substrate between the source and drain electrode where the gate electrode is formed using edge definition lithography. Claim 44 has been amended to recite that the gate electrode includes a first portion that extends outward from substrate and a second portion that extends in a direction transverse to the first portion and overhangs the substrate. Support for this amendment is found, for example, in Figures 5A-5C, which illustrate the formation of the gate electrode using edge definition lithography, Figures 9A-9D, which illustrate the outward extending and overhanging portion of the gate electrode, and on page 15, lines 1-15, which describe the formation of the gate electrode.

There is absolutely no disclosure, teaching, or suggestion in Danzilio or Lyons of a gate electrode with a first portion which extends outward from the substrate and a second portion that extends in a direction transverse to the first portion and overhangs the substrate where the gate electrode using edge definition lithography. In Lyons, the only structure formed using the lithographic technique described therein is a structure that extends outward from and does not overhang substrate **10**. Similarly, in Danzilio, gate electrode **411** extends outward from and does not overhang its substrate. Accordingly, it is respectfully submitted that the rejection of independent claim 44 and dependent claims 45-49 as unpatentable over Danzilio in view of Lyons should be withdrawn.

Claim 50

Claim 50 is rejected as unpatentable over U.S. Patent No. 4,400,865 to Goth et al. (hereinafter, "Goth") in view of Lyons. This rejection is respectfully traversed.

Claim 50 recites a bipolar junction transistor having a nanometer-scaled edge-defined feature. Claim 50 recites a collator layer, a base layer adjacent to the collector layer and a nanometer-scale emitter on the base layer using edge-definition lithography. Claim 50 has been amended to recite that the emitter extends outward from the base layer. Support for this amendment is found, for example, in Figures 10A-10C where emitter **1002** extends outward from base layer **1004**. There is absolutely no disclosure, teaching, or suggestion in Goth or Lyons of a bipolar junction transistor having a nanometer-scaled edge-defined emitter that extends outward from the base layer as claimed. Goth is the only document of these two that describes a bipolar junction transistor. However, in Figures 9A-9H of Goth relied upon in the official action, emitter **110** is surrounded by base region **80** and does not extend outward from base region **80**. Thus, when Goth is combined with Lyons as proposed in the official action, the result is an edge-defined emitter that is surrounded by the base region and that does not extend outward from the base region. Accordingly, it is respectfully submitted that the rejection of claim 50 as unpatentable over Goth in view of Lyons should be withdrawn.

Allowable Claims

Claims 41-43 were indicated as allowable. Claims 41-43 are rewritten in independent form to include all the elements of the base claim in any intervening claims. Accordingly, claims 41-43 should now be allowed.

Conclusion

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

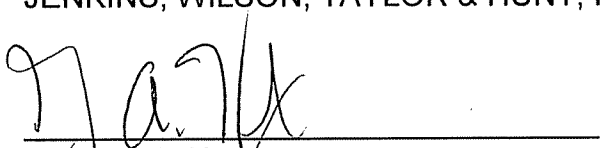
If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

The Commissioner is hereby authorized to charge the $995.00 fee for the filing of this Information Disclosure Statement, and any other fees associated with the filing of this document, to Deposit Account No. **50-0426**.

Respectfully submitted,

JENKINS, WILSON, TAYLOR & HUNT, P.A.

Date: November 17, 2008 By: 

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